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学 位 論 文 要 旨
Dissertation Summary

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論　文　名: Field Test for Ensuring the Functional Safety of Automotive System
(Dissertation Title)

Nowadays, with the rapid advances in automotive system, aircraft, intelligent transportation systems, the deep sub-micron devices that can achieve the high performance for dealing with the high-volume and complex data in the real time are required. On the other hand, ever-shrinking the features size of the deep sub-micron process make the devices embedded in such systems vulnerable to the aging phenomena, and when the devices work for a long time, the aging-induced faults would infringe on the reliability of the systems.

Field Testing is a promising way to detect the aging-induce faults by executing test while the system is in idle state, suspended or power-on/off, so as to ensure the system reliability. Power-On Self-Test (POST) is a well-known field-testing technique and has been applied to many systems that demand high reliability. Generally, the POST is executed during the start-up of the system to test the critical components of the system before starting any functional operations, thus the real-time state of the system including the aging-induced faults can be checked/detected in advance to avoid failures. However, POST suffers from a big challenge that is the time allowed for testing should be very limited (e.g.: <50ms for an automotive system). Thus, test data with large volume may be impossible to apply within the limited test time during the start-up of system. Moreover, depending on the system, POST is required to meet a target fault coverage which is usually very high, e.g.: in case of testing an automotive device, at least 90% fault coverage is required to comply with the requirement of ASIL D of the ISO26262 standard.

In order to implement the POST for an advance system, there are generally two strategies.

The first strategy refers to the Test Partitioning technology which divides the original large test set into some subsets with smaller volume to adapt with the limited test application time, and applies the test subsets every time when the system is starting up. The other one strategy refers to the Fault Detection Enhancement technology which focuses on reducing the test volume (test compression) to gain a target fault coverage, by improving the test quality of test patterns through the DFT (design for testability) technology.

In this study, we focus on the above two strategies to enable the application of POST in automotive system, and proposed the corresponding test techniques to improve the test quality of Test partitioning technology and the Fault Detection Enhancement technology, respectively.

Regarding the Test partitioning technology, the major problem of test partitioning is the Fault Coverage (FC) loss and the increase of detection latency of faults due to the missing test patterns of subsets. In this study, we proposed two approaches of test pattern partitioning to address these problems. In the first approach, we select the faults, which possibly has high aging speed as the ***risky faults***, and propose greedy pattern partitioning method to improve the detection latency and the fault coverage for the risky faults. In the second approach we utilize machine-learning techniques including the Simulated Annealing algorithm (SA) and Support Vector Machines model (SVM) for pattern partitioning aiming for achieving the optimal partitioning to minimize the detection latency (MTFD: Mean Time Fault Detection) of aging-induced faults. Experimental results on benchmark circuit demonstrated the effectiveness of the proposed approaches.

Regarding the Fault Detection Enhancement technology for POST, in this study we introduced the multi-cycle test to the logic built-in self-test (LBIST) scheme for reducing the volume of the root test data required for achieving a targeted high fault coverage specified by ISO26262 for automotive device testing. Since the multi-cycle test allows the test responses of the CUT (circuit under test) to be reused as test stimuli for testing that could detect additional faults before the following root test data is applied, it has promising potential to reduce the number of root test data for achieving a target fault coverage. However, we raise two major issues that obstruct the effect of multi-cycle test to reduce the root test data for shorting the test application time (TAT) of POST, which are Fault effects vanishing (FEV) problem and Fault Detection Degradation of capture patterns (FDD).

The Fault effects vanishing problem denotes the fault effects excited at some intermediate capture cycles might disappear before their effects are propagated to the final

capture cycle for observation due to the expanded long propagation path that would cause fault coverage loss. To address the FEV problem, we proposed a DFT technique named Fault-Detection-Strengthened (FDS) method for strengthening the fault detection capability of multi-cycle test by directly observing the values of small part of Flip-Flops (FFs) at each capture cycle. Also, we developed the underlying technologies including the FDS flip-flop (FF) design and an original in-house tool named FVP-TPI (Fault-effects-Vanishing Point-TPI) to compute the most effective insertion point of FDS_FFs. Experimental results of ITC99 benchmark circuits and the commercial circuits show significant fault coverage increase and large test data reduction for achieving 90% fault coverage that satisfies the requirement of functional safety by using small number of random root test data.

The Fault Detection Degradation (FDD) of capture patterns denotes the decrease of capability of capture pattern (the test responses of CUT) to detect more additional faults. To overcome the FDD problem, we proposed a DFT method named FF-Control Point Insertion (FF-CPI) technique by modifying the captured values of scan Flip-Flops (FFs) during capture operation. Also, we proposed the methods to evaluate the FFs for determining the candidate FFs for FF-CPI that can achieve more fault detection, by analyzing the circuit structure w/o any simulations for the purpose of shortening the development period of DFT. The Experimental results of benchmark circuits show that the proposed method can further reduce the number of root test data for achieving the specified target fault coverage compared to the FDS_FF method, which is helpful to further shorten the TAT of POST.